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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR  | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/765,631      | 01/27/2004  | Ghanashyam A. Bailwal | 15398US01           | 2270             |

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MCANDREWS HELD & MALLOY, LTD  
500 WEST MADISON STREET  
SUITE 3400  
CHICAGO, IL 60661

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| EXAMINER |
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STEELMAN, MARY J

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| ART UNIT | PAPER NUMBER |
|----------|--------------|

2191

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE  | DELIVERY MODE |
|--|------------|---------------|
| 3 MONTHS                               | 03/23/2007 | PAPER         |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/765,631

Applicant(s)

BAILWAL, GHANASHYAM A.

Examiner

Mary J. Steelman

Art Unit

2191

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 January 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. Claims 1-34 are pending.

#### ***Drawings***

2. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings are informal. Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

#### **INFORMATION ON HOW TO EFFECT DRAWING CHANGES**

##### **Replacement Drawing Sheets**

Drawing changes must be made by presenting replacement sheets which incorporate the desired changes and which comply with 37 CFR 1.84. An explanation of the changes made must be presented either in the drawing amendments section, or remarks, section of the amendment paper. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). A replacement sheet must include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of the amended drawing(s) must not be labeled as "amended." If the changes to the drawing figure(s) are not accepted by the examiner, applicant will be notified of any required corrective action in the next Office action. No further drawing submission will be required, unless applicant is notified.

Art Unit: 2191

Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and within the top margin.

### *Specification*

3. The use of the trademark 'Verilog / Microsoft Visual Studio' has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

See MPEP 7.35.01 Trademark or Trade Name as a Limitation in the Claim

Art Unit: 2191

Claims 1-34 contain the trademark/trade name JAVA. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe byte code programming language and, accordingly, the identification/description is indefinite.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-34 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent

Application Publication 2003/0061580 A1 to Greaves.

Per claim 1:

A method for translating Verilog into C++, the method comprising:

Art Unit: 2191

searching for a Verilog pattern in a Verilog file, the Verilog pattern associated with a specific functionality;

-substituting the Verilog pattern with a C++ language expression, wherein the C++ language expression is associated with the specific functionality.

Greaves: [0008]converting Verilog or VHDL to alternative programming languages such as C, C++... [0016], using a compiler [0021], hardware description language section is read...parsing...facilitate the conversion...into equivalent statements using a restricted subset of the language.

Per claim 2:

-the translating from Verilog into C++ utilizes macro functions in VBScript.

Greaves: [0024], separate modules must be written by a user to simulate such primitives found in the particular hardware description language...substitute user written modules

Per claim 3:

-identifying whether the Verilog file comprises at least one of a task library, a main driver, and a driver module.

Greaves: [0023], hardware description language section is flattened to create a single module from the modules, tasks, and functions that constitute the hardware description language section.

Root module calls sub modules (main driver).

Per claim 4:

Art Unit: 2191

-if the Verilog file comprises a task library: identifying a Verilog task within the task library; and translating the Verilog task into a C++ function;

-if the Verilog file comprises a main driver: inserting in the Verilog file at least one C++ interface header.

Greaves: [0023], tasks, driver module [0028], library of standard tasks and functions written in an object oriented programming language...substitute...for the task or function (of the HDL)...retrieve the mapto list and substitute...

Per claim 5:

-the Verilog pattern comprises # delay statements from the Verilog file.

Greaves: [0051], reserved words...require renaming...rules for renaming...prefixing one of a number of special strings. [0019], Expressions (# delay) are directly converted to the target alternative programming language.

Per claim 6:

-the Verilog pattern comprises 'ifdef statements in the Verilog file.

Greaves: [0051], reserved words...require renaming...rules for renaming...prefixing one of a number of special strings. [0019], Expressions ('ifdef) are directly converted to the target alternative programming language.

Art Unit: 2191

Per claim 7:

-the Verilog pattern comprises ' symbols from the Verilog file.

Greaves: [0051], reserved words...require renaming...rules for renaming...prefixing one of a number of special strings. [0019], Expressions (special symbols) are directly converted to the target alternative programming language.

Per claim 8:

-the Verilog pattern comprises a begin keyword in the Verilog file to a "{" symbol.

Greaves: See Table I, II, page 5.

Per claim 9:

-the Verilog pattern comprises an end keyword in the Verilog file to a "}" symbol.

Greaves: See Table I, II, page 5.

Per claim 10:

-the Verilog pattern comprises at least one register definition in the Verilog file into at least one C++ definition.

Greaves: As an example, see verilog code at [0063], including register definition

[0019], Expressions on the right hand side of each assignment statement are converted to use the set of operators found in the target language.



Art Unit: 2191

Per claim 11:

-the Verilog pattern comprises at least one combinatorial assignment in the Verilog file.

Greaves: [0036], combinatorial assignments

Per claim 12:

-the Verilog pattern comprises at least one event in the Verilog file into at least one C++ event.

Greaves: [0039], event condition

Per claim 13:

-the Verilog pattern comprises at least one Verilog switch in the Verilog file into at least one C++ switch.

Greaves: [0051], reserved words...require renaming...rules for renaming...prefixing one of a number of special strings. [0019], Expressions (switch) are directly converted to the target alternative programming language.

Per claim 14:

-the Verilog pattern comprises at least one Verilog concat expressions in the Verilog file into at least one C++ concat expressions.

[0051], reserved words...require renaming...rules for renaming...prefixing one of a number of special strings. [0019], Expressions (concat) are directly converted to the target alternative programming language.

Art Unit: 2191

Per claim 15:

-the Verilog pattern comprises at least one Verilog parameter in the Verilog file into at least one C++ #define.

Greaves: [0044], assignments are converted to variables that the alternative programming language can operate on.

Per claim 16:

-the Verilog pattern comprises at least one Verilog const in the Verilog file into at least one C++ const.

Greaves: [0048], define the parameters [0051], reserved words...require renaming...rules for renaming...prefixing one of a number of special strings. [0019], Expressions (const) are directly converted to the target alternative programming language.

Per claim 17:

-the Verilog pattern comprises at least one Verilog bit access macro in the Verilog file into at least one C++ functional equivalent.

Greaves: [0045], variable bit sizes

Regarding claims 18-34:

Claims are a "machine-readable storage having stored thereon, a computer program" version of claims 1-17 above. Rejection of limitations are as addressed above.

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Note prior art:

US Patent Application Publication 2003/0154464 A1 to Bollano et al.

VHDL automatically converted into a C++ model (Abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (571) 272-3704. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached at (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned: 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Art Unit: 2191

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman

03/08/2007

*Mary Steelman*  
*Primary Examiner*